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(74) Agents: **WILLIAMSON, Paul, L.** et al.; c/o Philips Intellectual Property, & Standards, Cross Oak Lane, Redhill Surrey RH1 5HA (GB).

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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

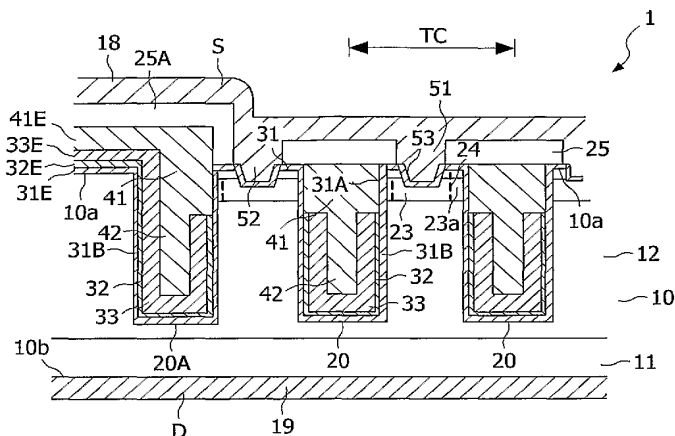
(75) Inventors/Applicants (for US only): **KOOPS, Gerrit, E., J.** [NL/BE]; c/o Philips Intellectual Property, & Standards, Cross Oak Lane, Redhill Surrey RH1 5HA (GB). **IN'T ZANDT, Michael, A., A.** [NL/NL]; c/o Philips Intellectual Property, & Standards, Cross Oak Lane, Redhill Surrey RH1 5HA (GB).

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(54) Title: TRENCH-GATE TRANSISTORS AND THEIR MANUFACTURE



(57) Abstract: A trench-gate transistor (1) has an integral first layer of silicon dioxide (31) which extends from the upper surface (10a) of the semiconductor body (10) over top corners of each cell array trench (20), the integral first layer also providing a thin gate dielectric insulating layer (31A) for a thick gate electrode (41) and the integral first layer also providing a first part (31B) of a stack of materials which constitute a thick trench sidewall insulating layer (31B, 32, 33) for a thin field plate (42), a layer of silicon nitride (32) providing a second part of the stack and a second layer of silicon dioxide (33) providing a third part of the stack. The integrity of the first silicon dioxide layer (31) over the trench (20) top corners helps to avoid gate (41) - source (24) short circuits. In a method of manufacture (Figures 2A to 2F) a hardmask (21) used to etch the trenches (20) is removed before providing the silicon dioxide layer (31), which layer (31) is then protected by successive selective etching of the oxide layer (33) and the nitride layer (32) in the upper parts of the trenches (20). After the gate electrodes (41) are provided, layers for the channel accommodating regions (23) and source regions (24) may be formed through the oxide layer (31) on the upper surface (10a).

**Declaration under Rule 4.17:**

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT,

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